

REMARKS/ARGUMENTS

This is in response to the Office Action dated March 22, 2004. Applicant amends claims 1, 7 and 11 and adds new claims 14-16. Applicant amends the drawings according to the Examiner's instructions. Reexamination and early favorable consideration are respectfully requested.

The Examiner requires that FIGS. 1-3 be designed with a legend as prior art. Applicant submits a proposed drawing amendment.

The Office Action rejects the pending claims over cited prior art, with U.S. Patent No. 6,319,784 to Yu, et al. (the Yu patent) as the primary reference. Applicant submits that the present claims distinguish over the art of record. The application is directed to preserving the integrity of silicon oxide shallow trench isolation structures and is particularly well suited to highly planar semiconductor processing techniques. These aspects of the disclosed method are emphasized in the present claims, which recite the formation of a protective film, where the top of the protective film is below other structures on the device being processed.

The present application discusses a problem that arises in forming self-aligned silicide ("salicide") contact structures in the presence of oxide shallow trench isolation structures. "Salicide" processing benefits from very clean silicon surfaces and the application describes using hydrofluoric acid or a similar cleaning solution to provide a clean silicon surface. Use of hydrofluoric acid or a similar cleaning solution can attack an oxide shallow trench isolation ("STI") structure, diminishing the reliability of the STI structure and, as another undesirable byproduct, leaving deposits on the surface of the device that can interfere with subsequent processing. The present application describes the use of a protective film to facilitate the more reliable use of hydrofluoric acid or similar cleaning solutions and to preserve STI structures formed before the cleaning.

In this, the present application stands in contrast to the cited Yu patent. The Yu patent seeks to avoid using “an HF dip or sputter etch” in favor of “H₂ annealing.” According to column 4, lines 14-16 of the Yu patent, use of the patent’s H₂ annealing allows the “HF dip [to] be eliminated resulting in a more environmentally friendly process.” Thus, the Yu patent teaches away from claim 1’s process of “cleaning a surface side of the semiconductor substrate with a cleaning solution” and refers to the HF dip only in explaining why the process is to be avoided.

The application describes forming the protective film in ways that facilitate planar processing. For example, the protective film 152 shown in FIG. 7 is formed in a limited fashion over the shallow trench isolation structure 102 and localized adjacent the gate electrodes 120, 122. This minimizes the extent of structure that needs to be planarized for effective subsequent processing. The process of forming the protective film also provides a reduced step between the STI structure and the gate electrodes. See application page 7, lines 15-22.

The improved planarity associated with the present invention is reflected in the now pending claims. For example, claim 1 recites “the top of the protective film is lower than the top of the semiconductor elements,” which reflects an aspect of the greater planarity achieved through practice of the claim 1 invention. These aspects of the present invention are not taught or suggested by the art of record to the present application.

The illustrations of the Yu patent illustrate the use of a local oxidation of silicon (“LOCOS”) process for forming field oxide (“FOX”). As is known in the art, the field oxide regions formed in this LOCOS process extends above the surface of the silicon substrate, typically on the order of thousands of Angstroms. The Yu patent later deposits a resist protection dielectric 26 (such as silicon oxide) and then

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forming openings in the resist protection dielectric 26 in which to form metal silicide regions on the source, drain and gate. The Yu patent tailors its process so that the resist protection dielectric 26 can be left in place, so that the resist protection dielectric is incorporated in the final device.

As shown in the illustrations, the result of the Yu patent's process is an elevated structure that can introduce difficulties into subsequent processing. For example, subsequent lithography steps have to be designed to provide sufficient depth of field to accommodate the elevated structure of the Yu patent.

Consequently the present claims distinguish over the teachings of the Yu patent. For example, claim 1 recites "the top of the protective film is lower than the top of the semiconductor elements." This does not happen with the Yu patent's process and so claim 1 and its dependent claims 2-7 distinguish over the Yu patent. It would not have been obvious to modify the Yu patent to address this deficiency, because any modification of the Yu patent would follow the Yu patent's teaching the "HF dip" or similar cleaning processes should be avoided. Any modifications to the Yu patent would similarly avoid practicing this aspect of the present invention.

The other claims recite similar limitations, which similarly are not taught or suggested by the Yu patent and the other prior art of record.

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6700 to discuss the steps necessary for placing the application in condition for allowance.

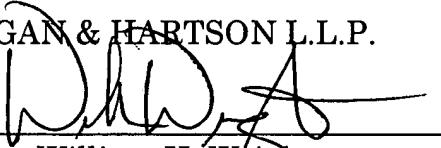
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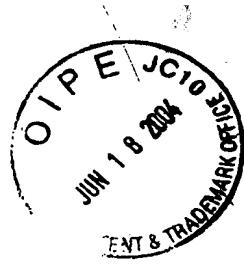
Respectfully submitted,

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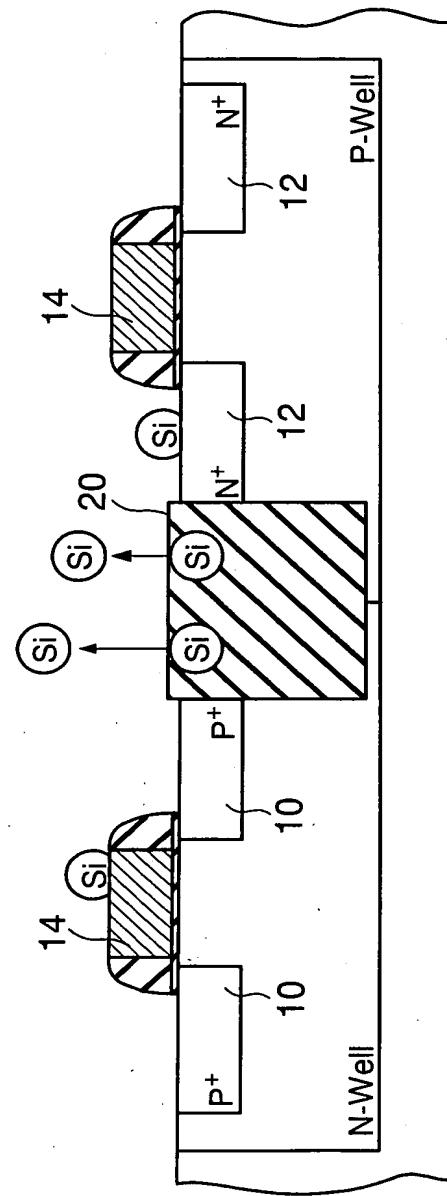


FIG. 1
PRIOR ART

Annotated Sheet Showing Changes

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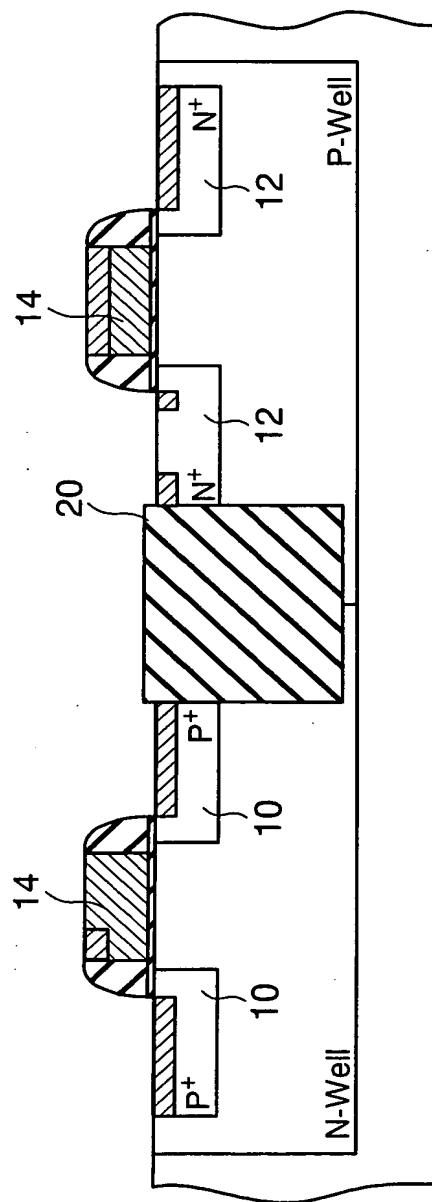


FIG.2
PRIOR ART

Applicant: Yasuo Okada
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Annotated Sheet Showing Changes

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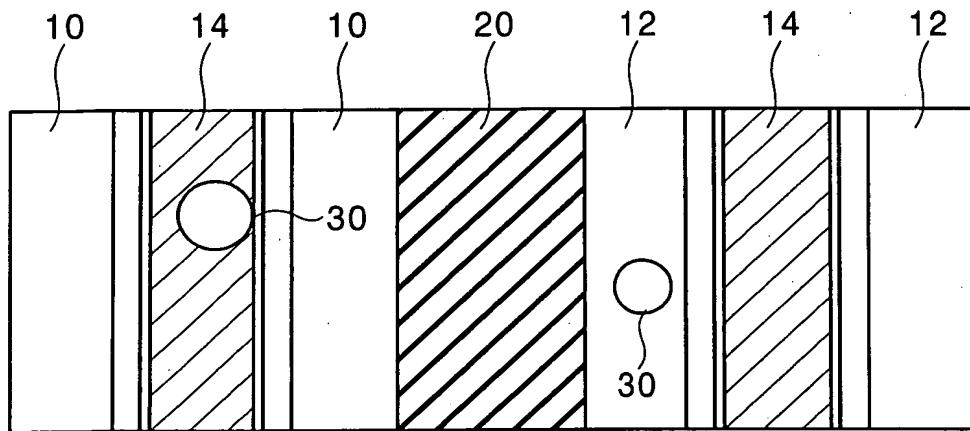


FIG.3

PRIOR ART